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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,753	07/01/2003	Bruce Gregory Warren	491442011600	5558

42178 7590 05/02/2008

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EXAMINER	
RUSSELL, WANDA Z	
ART UNIT	**PAPER NUMBER**
2616	
MAIL DATE	**DELIVERY MODE**
05/02/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/612,753	WARREN ET AL.	
	Examiner	Art Unit	
	WANDA Z. RUSSELL	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/18/2008 and 4/3/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/3/2008 has been entered.

Specification

2. The objection that the attorney's docket number should be removed from the specification has been withdrawn.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1 and 2** are rejected under 35 U.S.C. 103(a) as being unpatentable over Black et al. (U.S. Patent 6,614,796 B1), in view of Anderson et al. (U.S. Patent 6,898,184 B1).

For **claim 1**, Black et al. substantially teach a Fibre Channel Arbitrated Loop (Title) interconnect system (col. 1, lines 29-30) comprising:

a first port (108-Fig. 4, or 124-Fig. 5),

a second port (110-Fig. 4, or 126-Fig. 5),

the first and second ports including port logic to monitor certain arbitrated loop primitives (col. 15, line 4, and col. 14, lines 46-48),

a crossbar switch coupled to the first and second ports (100-Fig. 4),

a route determination apparatus (FCAL switch-Fig. 4, or 136-Fig. 5) including a routing table (127-Fig. 4), the route determination apparatus directly coupled to each port and the crossbar switch (Fig. 4 or Fig. 5, FCAL switch is directly connected to ports 108, 110 etc. in Fig. 4 or Fig. 5),

whereby the crossbar switch creates paths between the ports based on arbitrated loop primitives (col. 15, lines 2-4).

However, Black et al. fails to specifically teach ALPA addresses and their associated ports, and the routing table initialized with a device discovery process during loop initialization.

Anderson et al. teach ALPA addresses (col. 13, line 50) and their associated ports (col. 13, line 51), and the routing table initialized with a device discovery process during loop initialization (col. 13, lines 48-52).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Black et al. with Anderson et al. to obtain the invention for improving the routing process.

For **claim 2**, Black et al. and Anderson et al. teach everything claimed as applied above (see claim 1). In addition, Black et al. teach the interconnect system of claim l

whereby the arbitrated loop primitives that cause the crossbar switch to create paths between ports includes one or more of the following: ARB, OPN and CLS (col. 2, line 2).

5. **Claims 3-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Black et al. (U.S. Patent 6,614,796 B1), and further in view of Anderson et al. (U.S. Patent 6,898,184 B1), and Global Engineering ("Fibre Channel Arbitrated Loop" from IDS).

For **claim 3**, Black et al. substantially teach a Fibre Channel arbitrated loop (Title) interconnect system (col. 1, line 29-30), the interconnect system including:

a first port (124-Fig. 5) containing port logic (col. 8, line 14) coupled to the first Arbitrated Loop (Fig. 4, FCAL is Loop Switch),

a second port (126-Fig. 5) containing port logic (col. 8, line 14) coupled to the second Arbitrated Loop (Fig. 4, FCAL is Loop Switch),

route determination apparatus directly coupled to the first and second ports (FCAL switch-Fig. 4, or 136-Fig. 5. It is directly coupled to ports 108, 110 etc.) for selecting a route between ports (col. 14, lines 48-52), the route determination apparatus selecting (col. 15, line 4, and col. 14, lines 46-48) routes based on received Fibre Channel Arbitrated Loop primitives from the ports and including (127-Fig. 4) a routing table (127-Fig. 4) containing ALPA addresses and their associated ports (110, 112-Fig. 4),

connectivity apparatus (half bridges, 102-Fig. 4, and col. 14, line 12) directly coupled to the first and second ports and to the route determination apparatus for

switching frames (col. 1, line 20) between ports under control of the route determination apparatus,

wherein the connectivity apparatus is a crossbar switch (Fig. 4 and 5), and

wherein Fibre Channel frames (col. 1, line 20) are transferred between a device on the first Arbitrated Loop and the second Arbitrated Loop Device (source and destination, col. 1, lines 20-27).

However, Black et al. fails to specifically teach a system for interconnecting Fibre channel Arbitrated Loop devices comprising: a first Arbitrated Loop containing one or more Fibre Channel arbitrated loop devices, and a second Arbitrated Loop Device, and ALPA addresses and the routing table initialized with a device discovery process during loop initialization.

Global Engineering teaches

a system (Fig. J.1, P. 122) for interconnecting Fibre channel Arbitrated Loop devices (Fig. J.1, P. 122) comprising:

a first Arbitrated Loop containing one or more Fibre Channel arbitrated loop devices (right side of Fig. J.1, P. 122 with the fabric element),

a second Arbitrated Loop (right side of Fig. J.1, P. 122 with the second Fabric Element-Fig. J.1, P. 122); and

Anderson et al. teach ALPA addresses (col. 13, line 50) and the routing table initialized with a device discovery process during loop initialization (col. 13, lines 48-52).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Black et al. with Anderson et al., and

Global Engineering to obtain the invention as specified in claim 3 for supporting more users for the system and improving the routing process.

For **claim 4**, Black et al., Anderson et al. and Global Engineering teach everything claimed as applied above (see claim 3). In addition, Black et al. teach the interconnect system of claim 3 whereby the arbitrated loop primitives that cause the crossbar switch to create paths between ports includes one or more of the following: ARB, OPN and CLS (col. 2, line 2).

For **claim 5**, Black et al., Anderson et al. and Global Engineering teach everything claimed as applied above (see claim 3). In addition, Black et al. teach the interconnect system of claim 3 including a R_RDY (col. 1, line 26) counter to count R_RDY's before the OPN response is received by the originating Fibre Channel Arbitrated Loop Device that is connected to the interconnect system (col. 1, lines 24-26).

For **claim 6**, Black et al. substantially teach a system (FCAL nets, col. 10, line 22) for interconnecting Fibre Channel Arbitrated Loop devices (Fig. 4) comprising:

a first Fibre Channel Arbitrated Loop Switch (Fig. 4, and col. 10, line 22. More nets can use more switches),

a second Fibre Channel Arbitrated Loop Switch (Fig. 4, and col. 10, line 22),

the first and second Fibre Channel Arbitrated Loop Switches including port logic (col. 8, line 14), connectivity apparatus (102, 104, 106-Fig. 4) and route determination logic (127-Fig. 4), the route determination logic directly coupled to the port logic and the connectivity apparatus (Fig. 4), and

a route determination logic creating routes based on the receipt of certain arbitrated Loop primitives (col. 15, lines 2-4),

wherein the first and second loop switches are interconnected by two or more Fibre Channel Arbitrated Loop links (col. 2, line 60) and transfer frames on both ports (col. 1, line 20).

However, Black et al. fail to specifically teach a system for interconnecting Fibre channel Arbitrated Loop devices comprising: a first Arbitrated Loop containing one or more Fibre Channel arbitrated loop devices, and a second Arbitrated Loop Device, and the routing table initialized with a device discovery process during loop initialization.

Global Engineering teaches a system (Fig. J.1, P. 122) for interconnecting Fibre channel Arbitrated Loop devices (Fig. J.1, P. 122) comprising:

a first Fibre Channel Arbitrated loop switch (X-Fig. Q. 1, P. 132),

a second Fibre Channel Arbitrated loop switch (Y-Fig. Q. 1, P. 132); and

Anderson et al. teach the routing table initialized with a device discovery process during loop initialization (col. 13, lines 48-52).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine [Black et al.] with [Global Engineering] to obtain the invention as specified in claim 6 for supporting more users for the system and improving the routing process.

For **claim 7**, Black et al. substantially teach a system comprising:

a plurality of Fibre Channel Arbitrated Loop ports (108, 110-Fig. 4) each including port logic (col. 8, line 14),

a route determination apparatus (FCAL switch-Fig. 4, or 136-Fig. 5) comprising a routing table (127-Fig. 4),

a crossbar switch (100-Fig. 4) adapted to connect the Fibre Channel Arbitrated Loop ports based on the receipt of certain Fibre Channel Arbitrated Loop primitives (col. 15, line 4, and col. 14, lines 46-48),

wherein a LIP received on the first port is selectively propagated to one or more of the ports (col. 42, lines 14-18), and

wherein the route determination apparatus is directly coupled to the plurality of ports and the crossbar switch (Fig. 4).

However, Black et al. fail to specifically teach a system for interconnecting Fibre channel Arbitrated Loop devices, and the routing table initialized with a device discovery process during loop initialization.

Global Engineering teaches a system (Fig. J.1, P. 122) for interconnecting Fibre channel Arbitrated Loop devices (Fig. J.1, P. 122); and

Anderson et al. teach and the routing table initialized with a device discovery process during loop initialization (col. 13, lines 48-52).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine [Black et al.] with [Global Engineering] to obtain the invention as specified in claim 6 for supporting more users for the system and improving the routing process.

For **claim 8**, Black et al. substantially teach a system for interconnecting Fibre Channel Arbitrated Loop Devices comprising:

a plurality of Fibre Channel Arbitrated Loop ports (108, 110-Fig. 4) each including port logic (col. 8, line 14),

a route determination apparatus (FCAL switch-Fig. 4, or 136-Fig. 5) comprising a routing table (127-Fig. 4),

the routing table initialized with a device discovery process during loop initialization,

a connectivity apparatus (half bridges, 102-Fig. 4, and col. 14, line 12), and

logic (col. 8, line 14) implementing predefined loop control criteria to enforce fairness (col. 8, lines 14-18).

However, Black et al. fail to specifically teach a system for interconnecting Fibre channel Arbitrated Loop devices, and the routing table initialized with a device discovery process during loop initialization.

Global Engineering teaches a system (Fig. J.1, P. 122) for interconnecting Fibre channel Arbitrated Loop devices (Fig. J.1, P. 122); and

Anderson et al. teach and the routing table initialized with a device discovery process during loop initialization (col. 13, lines 48-52).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine [Black et al.] with [Global Engineering] to obtain the invention as specified in claim 6 for supporting more users for the system and improving the routing process,

wherein the route determination apparatus is directly coupled to the plurality of ports and the connectivity apparatus (Fig. 4).

For **claim 9**, Black et al., Anderson et al. and Global Engineering teach everything claimed as applied above (see claim 8). In addition, Black et al. teach a system for interconnecting Fibre Channel Arbitrated Loop Devices of claim 8, wherein the fairness logic serves to limit the number of times a connected device opens another device (col. 1, line 32, and 29-32).

For **claim 10**, Black et al., Anderson et al. and Global Engineering et al. teach everything claimed as applied above (see claim 8 and 9). In addition, Black et al. teach a system for interconnecting Fibre Channel Arbitrated Loop Devices of claim 9, wherein the fairness logic serves to limit the number of times a connected device sequentially opens another device (col. 35, lines 21-24).

For **claim 11**, Black et al., Anderson et al. and Global Engineering teach everything claimed as applied above (see claim 8). In addition, Black et al. teach a system for interconnecting Fibre Channel Arbitrated Loop Devices of claim 8, further including a counter to count the number of opens (col. 44, line 33).

For **claim 12**, Black et al., Anderson et al. and Global Engineering teach everything claimed as applied above (see claim 8 and 11). In addition, Black et al. teach a system for interconnecting Fibre Channel Arbitrated Loop Devices of claim 11, wherein the counter counts sequential opens (col. 44, lines 45-48).

For **claim 13**, Black et al., Anderson et al. and Global Engineering teach everything claimed as applied above (see claim 8). In addition, Black et al. teach a system for interconnecting Fibre Channel Arbitrated Loop Devices of claim 8, wherein the logic proactively closes a device (col. 23, line 16).

For **claim 14**, Black et al., Anderson et al. and Global Engineering teach everything claimed as applied above (see claim 8). In addition, Black et al. teach a system for interconnecting Fibre Channel Arbitrated Loop Devices of claim 8, wherein the ports are assigned different access priorities (col. 7, line 37).

Response to Amendment

6. Applicant's amendment filed 4/3/2008 has been received and considered.

Response to Arguments

7. Applicant's arguments with respect to claim(s) 1-14 have been considered but they are not persuasive.

8. Applicant argues that the route determination apparatus is not directly connected to each port.

In response, the Examiner respectfully disagrees.

The route determination apparatus, FCAL switch, not the routing table, in Fig. 4 is directly connected to ports 108, 110 etc.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WANDA Z. RUSSELL whose telephone number is (571)270-1796. The examiner can normally be reached on Monday-Thursday 9:00-6:00 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Seema Rao can be reached on (571) 272-3174. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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